

*National University of Computer & Emerging Sciences Islamabad*

***Name: Muhammad Ahmed Baig***

***Roll #: 20i-1884***

***Section: BS(CS)-B***

### Title:

Flip Flops and Counters

### Objectives:

* Getting familiar with characteristic tables and characteristic functions of flip-flops
* Gaining a close insight into the functioning and properties of basic static memory circuits
* Developing skills in the composition and testing of sequential logic circuits.

### Equipment Required:

* + DEV-2765E Trainer Board
  + 7474 Dual +ve edge triggered D-Flip Flop
  + 74112 Dual –ve edge triggered JK-Flip Flop

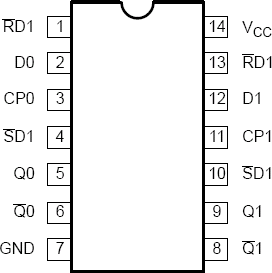
**Flip Flops**

A flip-flop is usually constructed by combining two same or different types of latches. Flip-flop circuits are constructed in such a way as to make them operate properly when they are a part of a sequential circuit that employs a single clock. Note that the problem with the latch is that as soon as an input changes, shortly thereafter the corresponding output changes to match it. This is what allows a change on a latch output to produce additional changes at other latch outputs while the clock pulse is at logic 1. The key to the proper operation of flip-flops is to prevent them from being transparent. In a flip-flop, before an output can change, the path from its inputs to its outputs is broken. So a flip-flop cannot “see” the change of its output or of the outputs of other, like flip-flops at its input during the same clock pulse. Thus, the new state of a flip-flop depends only on the immediately preceding state, and the flip-flops do not go through multiple changes of state. The edge triggered D flip flop avoids the problem of the RS invalid output states by not allowing the invalid states. The JK flip flop is a clocked RS flip flop with additional logic to replace the RS invalid output states with a new mode called toggle. Toggle causes the flip flop to change to the state opposite to its present state.

**D-Flip Flop**

### Pin Configuration of 7474 (D-FFP):

Vcc GND

D

CP

Set Reset

D

CP

Set Reset

Q

Q

Q

8

9

12

11

10

13

6

5

2

3

4

1

7

14

Q

7474

## Description of PINS

The 7474 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set (SD) and reset (RD) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and Q outputs on the low-to-high transition of the clock

## Function Table:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | **OUTPUTS** | | **OPERATING MODE** |
| **SD** | **RD** | **CP** | **D** | **Q** | **~Q** |
| 0 | 1 | X | X | 1 | 0 | Asynchronous set |
| 1 | 0 | X | X | 0 | 1 | Asynchronous reset |
| 0 | 0 | X | X | 1 | 1 | Undetermined\* |
| 1 | 1 | ↑ | 1 | 1 | 0 | Load “1” |
| 1 | 1 | ↑ | 0 | 0 | 1 | Load “0” |
| 1 | 1 | 1 | X | NC | NC | Hold |

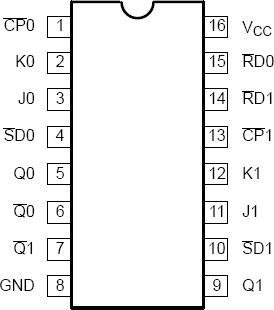
### Procedure

1. Connect the trainer with the power supply
2. Mount the IC 74LS74 on the trainer board
3. Supply the VCC and GND to the pin 16 and 8 respectively
4. Connect only one of the two flip-flops available on the IC. The pin configuration and characteristic table (function table) for this IC is given above.
5. Drive the D input with input switch on the trainer board and CP input from the clock on the trainer board. Connect output Q0 & ~ Q0 with LED.
6. Be sure to connect the set (SD) and reset (RD) inputs to a logical 1.
7. Using the different input combinations and verify the D flip-flop characteristic table.
8. Observe and record the output on the LED.

## JK- FLIP FLOP

### Pin Configuration of 74112 (JK-FFP):

Vcc GND

J K CP

Set

Reset

J K CP

Set

Reset

Q

Q

Q

7

9

11

12

13

10

14

6

5

3

2

1

4

15

8

16

Q

74112

## Description of PINS:

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, feature individual J, K, Clock (CPn), Set (SD) and Reset (RD) inputs, true (Qn) and complementary (~Qn) outputs. The SD and RD inputs, when Low, set or reset the outputs as shown in the Function Table, regardless of the level at the other inputs. A High level on the clock (CPn) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the CPn is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the CPn.

## Function Table:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | | **OUTPUTS** | | **OPERATING MODE** |
| **SD** | **RD** | **CP** | **J** | **K** | **Q** | **Q** |
| 0 | 1 | X | X | X | 1 | 0 | Asynchronous Set |
| 1 | 0 | X | X | X | 0 | 1 | Asynchronous Reset |
| 0 | 0 | X | X | X | 1\* | 1\* | Undetermined \* |
| 1 | 1 | ↓ | 1 | 1 | ~q | q | Toggle |
| 1 | 1 | ↓ | 0 | 1 | 0 | 1 | Load “0” (Reset) |
| 1 | 1 | ↓ | 1 | 0 | 1 | 0 | Load “1” (Set) |
| 1 | 1 | ↓ | 0 | 0 | q | q | Hold “no change” |
| 1 | 1 | 1 | X | X | Q | Q | Hold “no change” |

\* = Both outputs will be High while both SD and RD are Low, but the output states are unpredictable if SD and RD go High simultaneously.

### Procedure

1. Connect the trainer with the power supply
2. Mount the IC 74LS112 on the trainer board
3. Supply the VCC and GND to the pin 16 and 8 respectively
4. Connect only one of the two flip-flops available on the IC. Refer to the pin configuration and characteristic table (function table) for this IC is given above.
5. Drive the J, K and CK inputs input switch on the trainer board and CP input from the clock on the trainer board. Connect output Q0 & ~Q0 with the LED.
6. Be sure to connect the set (SD) and reset (RD) inputs to a logical 1.
7. Using the different input combinations, verify the JK flip-flop characteristic table.
8. Observe and record the output on the LED.

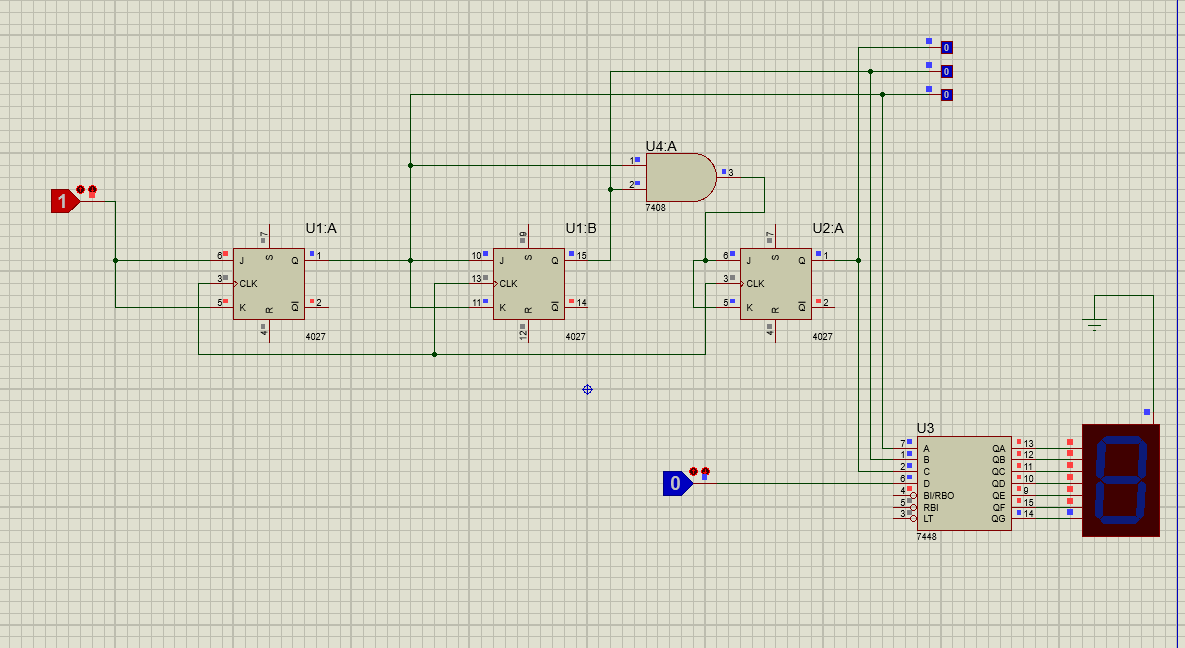
## Counters

A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses may be clock pulses or may originate from some other source, and they may occur at fixed intervals of time or random intervals. The sequence of states may follow the binary number sequence or any other sequence of states: A counter that follows the binary number sequence is called a binary counter.

Counters are available in two categories: ***ripple counters and synchronous counters***. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip-flops. In other words, the clock inputs of some or all of the flip-flops are triggered not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs. In a synchronous counter, the clock inputs of all of the flip-flops receive the common clock pulse, and the change of state is determined from the present state of the counter.

## Asynchronous Counter

**Block Diagram:**



**Synchronous Counter (Up/Down)**

**Block Diagram:**

